Agilent Technologies Z5623A Option K64

User's and Service Guide

Use this manual with the following documents:

PNA Series Network Analyzer On-line Help System

Application Note 1408-12

Agilent Technologies

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WARNING	**Warning denotes a hazard. It calls attention to a procedure which, if not correctly performed or adhered to, could result in injury or loss of life. Do not proceed beyond a warning note until the indicated conditions are fully understood and met.**

CAUTION	Caution denotes a hazard. It calls attention to a procedure that, if not correctly performed or adhered to, could result in damage to or destruction of the instrument. Do not proceed beyond a caution sign until the indicated conditions are fully understood and met.

Statement of Compliance

This product has been designed and tested in accordance with the standards listed on the Manufacturer's Declaration of Conformity, and has been supplied in a safe condition. The documentation contains information and warnings that must be followed by the user to ensure safe operation and to maintain the product in a safe condition.

Definitions

- *Specifications* describe the performance of parameters covered by the product warranty (temperature – 0 to 55 °C, unless otherwise noted.)
- *Typical* describes additional product performance information that is not covered by the product warranty. It is performance beyond specification that 80% of the units exhibit with a 95% confidence level over the temperature range 20 to 30 °C. Typical performance does not include measurement uncertainty.
- *Nominal* values indicate expected performance, or describe product performance that is useful in the application of the product, but is not covered by the product warranty.

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Z5623A Option K64

Description

The Agilent Z5623AK64 is a 10 MHz to 20 GHz High Power Test Set. When connected to the N5230A 4-Port PNA-L Series Network Analyzer. High power forward direction measurements can be made from Test Port 5 to Port 6.

The Z5623AK64 can be configured in several ways. The Test Set Bypass configuration allows the user to use N5230A 4-Port PNA-L Series Network Analyzer from 10 MHz to 20 GHz in its normal mode. This mode bypasses the Test Set's internal couplers through solid-state switches. The performance of Ports 1 and 4 of the N5230A 4-Port PNA-L Series Network Analyzer are degraded due to cable and switch loss in the Test Set. In the High Power mode the Test Set can be configured for specific application needs by the insertion of high power amplifiers, attenuators, isolators and other signal conditioning accessories. This will allow high power measurements at RF levels up to 20 Watts (+43 dBm) from 10 MHz to 20 GHz.

The N5230A rear panel Test Set I/O 25 pin D-sub connector controls the Z5623AK64 High Power Test Set. The N5230A 4-Port PNA-L Series Network Analyzer has an Interface Control panel that will allow the user to send address and data to the High Power Test Set. Information about the Interface Control can be found in the PNA on line help menu under Interface Control. N5230A PNA-L Series Network Analyzer information, Data sheets, white papers, or manuals can be viewed or printed by visiting our web site at http://www.agilent.com/find/pna.

The High Power configuration requires an amplifier, attenuators, and isolator and that is connected to the Test Set's front panel access source and receiver ports to protect the test set and network analyzer. Agilent does not supply these accessories with the Z5623AK64.

Currently the PNA using the Interface Control only supports a Thru Response Calibration in the High Power mode.

The Test Set is shipped from the factory with jumper cables installed on the front.

Content List

Agilent Part Number	Description	Qty
5023-0132	Locking Feet (set)	1
5063-9228	Front Handle Kit	1
5063-9235	Rack Mount Kit	1
8120-6818	Test Set I/O Cable	1
E8356-20072	Front Panel RF Access Jumpers	5
Z5623-20418	Short Interconnect RF Access Jumpers	5
Z5623-20419	Long Interconnect RF Access Jumpers	5
Z5623-90074	User's and Service Guide	1

General Specifications

Power Requirements

Verify that the required ac power is available at all necessary locations before installing the Test Set to the PNA.

- Three-wire power cables (which provide a safety ground) must be used with all instruments.
- Air-conditioning equipment (or other motor-operated equipment) should not be placed on the same ac line that powers the Test Set and PNA.
- Table 1 contains the maximum VA rating and BTU/hour rating for all instruments. This table can be use to determine the electrical and cooling requirements.

NOTE Values are based on 120 Vac supplied to each instrument at 60 Hz.

Table 1 Power Requirements

Standard Equipment		
Instrument	**Maximum VA Rating**	**Maximum BTU/Hour**
N5230A	350	1195
Z5623AK64	320	1095
Total	670	2290

Environmental Requirements

The environmental requirements of the system are listed in Table 2. Note that these requirements are the same as those of the N5230A Network Analyzer with Option 245.

Table 2 Operating Environment

Temperature	
Operation	5 °C to 40 °C (41 °F to 104 °F)
Storage	–40 °C to +65 °C (–40 °F to +158 °F)
MeasurementCalibration	20 °C to 26 °C (68 °F to 79 °F)
PerformanceVerification	Temperature must be within 1 °C (1.8 °F) of the temperature at which the measurement calibration was performed.
Relative Humidity	
Operation	5% to 95% at 40 °C or less (non-condensing)
Storage	5% to 95% at 65 °C or less (non-condensing)
Pressure Altitude (Operation or Storage)	Less than 3000 meters (~ 9,800 feet)

Environmental Tests

The Z5623AK64 complies with all applicable safety and regulatory requirements for the intended location of use and have been evaluated to assure that they are consistent with Agilent quality and reliability goals. On the basis of that evaluation, the following environmental tests have been deemed unnecessary and have not been performed: temperature, humidity, shock, vibration, altitude and power line conditions.

Equipment Heating and Cooling

If necessary, install air conditioning and heating to maintain the ambient temperature within the appropriate range. Air conditioning capacity must be consistent with the BTU ratings given in Table 1.

Required Conditions for Accuracy Enhanced Measurement

Accuracy-enhanced (error-corrected) measurements require the ambient temperature of the PNA and Test Set to be maintained within ± 1 °C of the ambient temperature at calibration.

Dimensions and Space Requirements

Standard installation of the Z5623AK64 and PNA includes configuration and installation on a customer provided lab bench or table top of adequate size and strength.

Table 3 System Dimensions

Item	Weight
Required Bench Top Dimension:	
Clearance above the bench	43 cm (17 in)
Width	127 cm (50 in)
Depth	102 cm (40 in)
Weight	55 kg (110 lb)

Table 4 Instrument Dimensions

Model	Weight	Height	Width	Depth
N5230A	24.9 kg, 55 lb. (± 0.5 lb.)	26.7 cm (10.5 in)	42.5 cm (16.7 in)	42.6 cm (16.8 in)
Z5623AK64	9.1 kg (20 lb.)	19.1 cm (7.5 in)	42.5 cm (16.7 in)	42.6 cm (16.8 in)

DUT Control Limits

Table 5 Control Limits

Item	Specifications
Connector Shape	15-pin female D-Sub
Voltage Range:	
Positive Input	0 to +5 V
Negative Input	–5 to 0 V
Maximum Current	100 mA in total of each line
Impedance	< 10 Ω
Range of Variable Voltage	+2 to +5 V

Maximum Power Levels

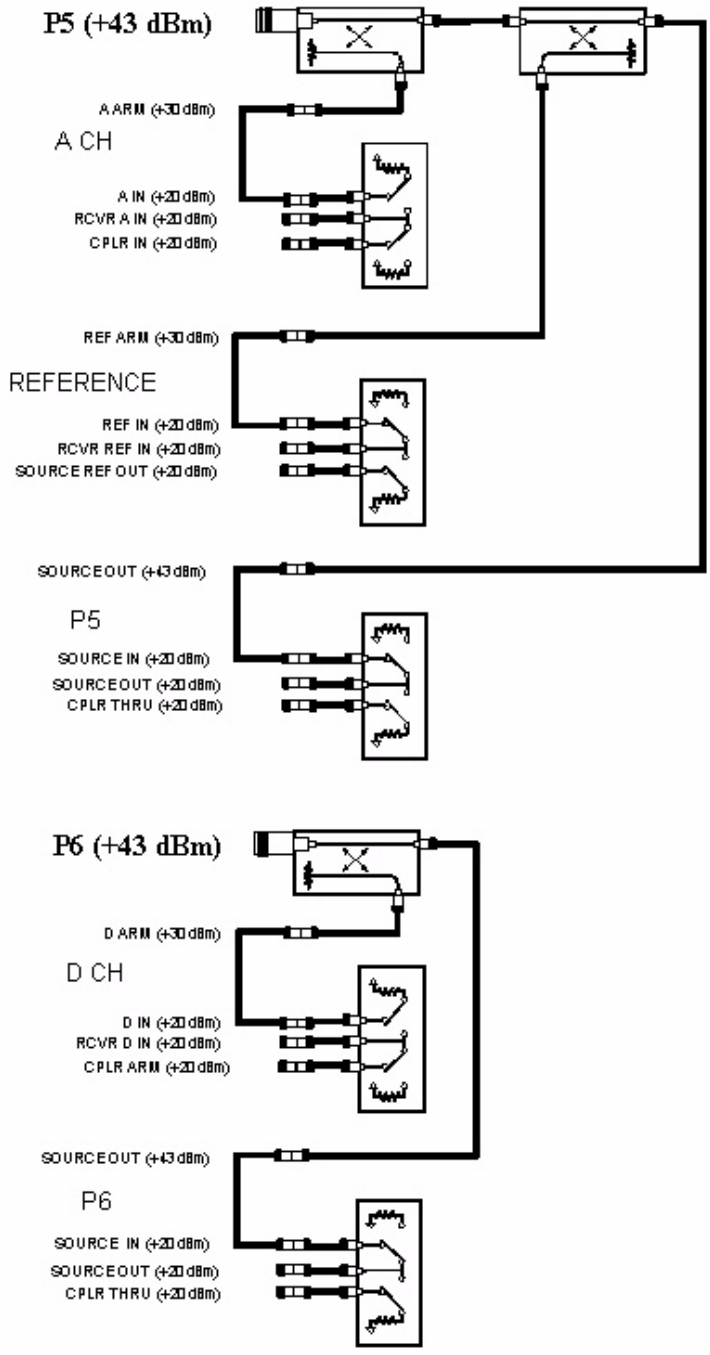
CAUTION It is recommend that you do not operate components near damage or maximum levels. The power levels should be kept at less than 3 dB, preferably 6 dB, below damage and maximum levels.

Table 6 Power Levels

Test Setup	Power Level
Maximum Z5623AK64 RF Power Levels for Access and Test Ports:	
SOURCE REF OUT, RCVR REF IN	+20 dbm 0 VDC
REF IN	+20 dBm 0 VDC
REF ARM	+30 dbm 0 VDC
SOURCE P5 IN	+20 dBm 0 VDC
SOURCE P5 OUT	+43 dbm 0 VDC
A IN	+20 dBm 0 VDC
A ARM	+30 dbm 0 VDC
CPLR ARM, RCVR A IN	+20 dBm 0 VDC
SOURCE OUT, CPLR THRU	+20 dbm 0 VDC
SOURCE P6 IN	+20 dBm 0 VDC
SOURCE P6 OUT	+43 dbm 0 VDC
D IN	+20 dBm 0 VDC
D ARM	+30 dbm 0 VDC
CPLR ARM, RCVR D IN	+20 dBm 0 VDC
SOURCE OUT, CPLR THRU	+20 dbm 0 VDC
Test Ports 5 and 6	+43 dBm 0 VDC
Maximum PNA-L RF Power Levels to Access and Test Ports:	
Max Recommended RF Level at A/B/C/D/R Receivers	–15 dbm
Damage Level at A/B/C/D/R Receivers	+15 dbm
Max Recommended RF Level at Port 1, 2, 3, 4 Source	+0 dBm
Damage Level to Port 1, 2, 3, 4 Source Out	+20 dBm
Max Level to Port 1, 2, 3, 4 Test Ports	+20 dBm

NOTE Refer to your PNA-L specifications to optimize the power levels in the receivers.

Figure 1 Signal Path Power Levels



Operation

The Agilent Z5623AK64 High Power Test Set can be configured for many applications. Included in this document are three typical configurations:

- Agilent Z5623AK64 Shipped Configuration, see Figure 2 on page 11.
- Agilent Z5623AK64 Setup Configuration, see Figure 9 on page 17.
- Agilent Z5623AK64 High Power Configuration, see Figure 10 on page 18.

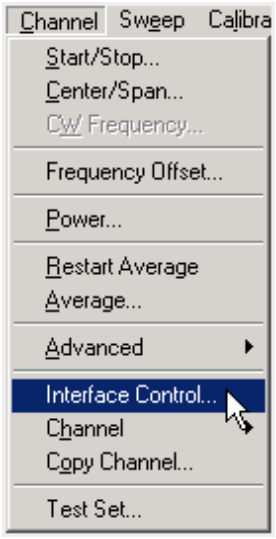
NOTE The internal firmware of the Agilent N5230A 4-Port PNA-L Series Network Analyzer has not been modified for this test set option. Power levels may differ from those indicated on the PNA when the Test Set is connected.

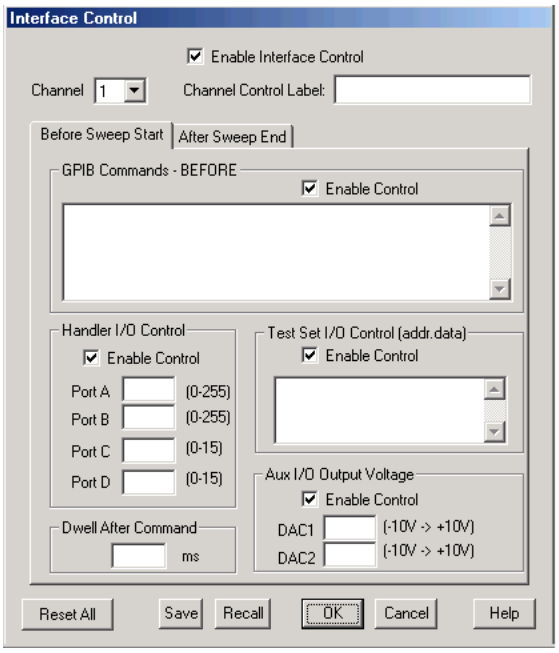
NOTE Refer to the enclosed configuration diagrams for external component connections and/or operating constraints when utilizing the high power capability of the Z5623AK64. External components are not supplied with the Z5623AK64 High Power Test Set.

CAUTION The Z5623AK64 High Power Test Set is equipped with receiver access ports. The jumpers can be removed to insert attenuators that will reduce the RF power to the PNA-L A,B and R channel receivers. Recommended power levels to the PNA-L receiver ports is –15 dBm. Refer to your PNA-L specifications to optimize power levels to the receiver ports.

CAUTION Prior to powering-up the booster amplifier it is highly recommended that the user verify the RF power levels seen by the various elements of the test setup. Both the PNA and Test Set power levels must be taken into consideration. At high power levels, a mistake could permanently damage the instruments. Accordingly, the following key values are given in Figure 1 on page 8 and Table 6 on page 7.

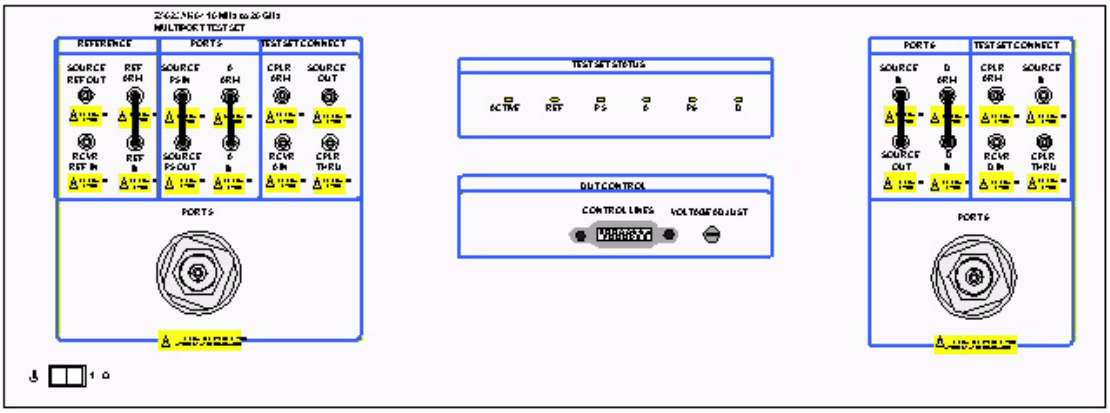
NOTE The N5230A 4-Port PNA-L Series Network Analyzer comes with the Interface Control application. Please review this application before connecting the Z5623AK64 Test Set to the PNA. Information regarding this application can be found in the PNA's Help Menu under "Interface Control". The application is shown below.





Z5623AK64 High Power Test Set

Figure 2 Front Panel (High Power Test Set)



Test Set Status LEDs

ACTIVE - On = the Test Set is being addressed. Off = Test Set is *not* being addressed.

REF - On = the Test Set reference is in use. Off = the reference is set to the PNA.

P5 - On = the Source is connected to Port 5. Off = the Source is connected to Port 1 of the PNA.

A - On = A Channel is connected to Port 5. Off = A Channel is connected to Port 1 of the PNA.

P6 - On = the Source is connected to Port 6. Off = the Source is connected to Port 4 of the PNA.

D - On = D Channel is connected to Port 6. Off = A Channel is connected to Port 4 of the PNA.

Reference Access Ports - SMA (female)

SOURCE REF OUT - Receives PNA Reference Source.

RCVR REF IN - Output for PNA Reference Receiver.

REF ARM - Test Set's Reference Output from Reference Coupler.

REF IN - Test Set's Reference Input to Reference Switch.

Port 5 Access Ports - SMA (female)

SOURCE IN - Source from PNA.

SOURCE OUT - Source to Test Port 5.

A ARM - Tests Set's A Channel Output from A Channel Switch.

A IN - Input to A Channel Switch.

Test Set Connector Access Ports - SMA (female)

CPLR ARM - A Channel Input from PNA port 1.

RCVR A IN - A Channel Output from Test Set A Channel switch.

SOURCE OUT - Test Port 1 Source Input from PNA.

CPLR THRU - Source Output to PNA Port 1 from Test Set Port 5 switch.

Test Ports - 3.5 mm Bulkhead Test Ports (male)

PORT 5 - Incident High Power Port

PORT 6 - Receive High Power Port

Line Switch

Standby - OFF

1 - ON, Power LED On

DUT Control

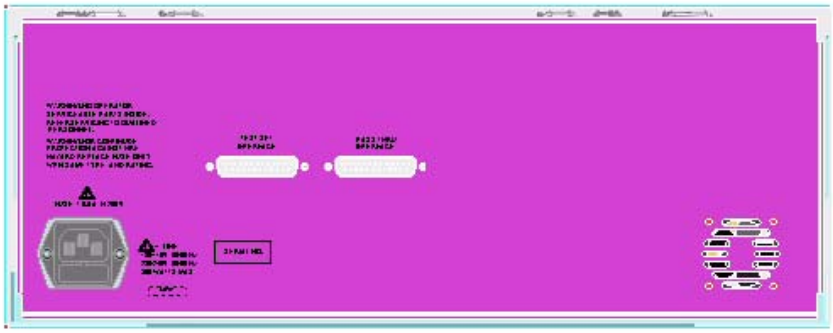
CONTROL LINES - 8 Lines that can supply voltage to assist in controlling a DUT.

VOLTAGE ADJUST - Adjustment resistor to vary Pin 12 of the DUT CONTROL from 2 to 5 volts.

Line Module

The line fuse, as well as a spare, reside within the line module. Figure 3 illustrates where the fuses are located and how to access them.

Figure 3 Rear Panel (High Power Test Set)



Available Fuses

- **United States (115 V orientation)**
  Fuse (F 5 A/250V, 2110-0709) U.L. listed and CSA certified
- **Europe (230 V orientation)**
  Fuse (F 5.0A/250V, 2110-0709) IEC listed and U.L. recognized certified

WARNING **For continued protection against fire hazard replace line fuse only with same type and rating:**
• United States—F 5A/250V, Part Number 2110-0709
• Europe—F 5A/250V, Part Number 2110-0709
The use of other fuses or material is prohibited.

Figure 4 Line Fuse

Test Set Interface

Connection to the PNA Test Set I/O connector or from Pass Thru Interface from another Test Set.

Pass Through Interface

Connection to another Test Set's, Test Set Interface.

System Setup

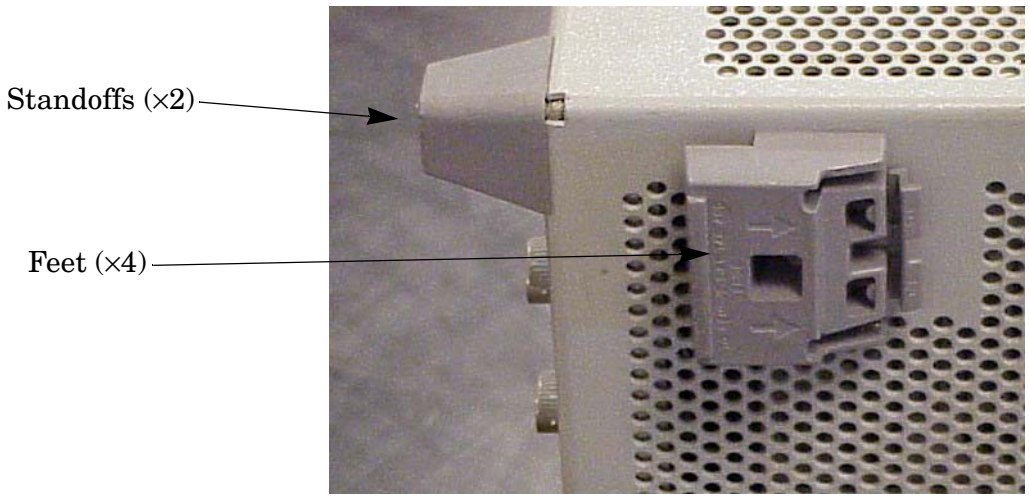
Attaching the Test Set to the PNA

This step is not necessary if you plan to place the Network Analyzer and Test Set in an equipment rack.

Preparing the Network Analyzer

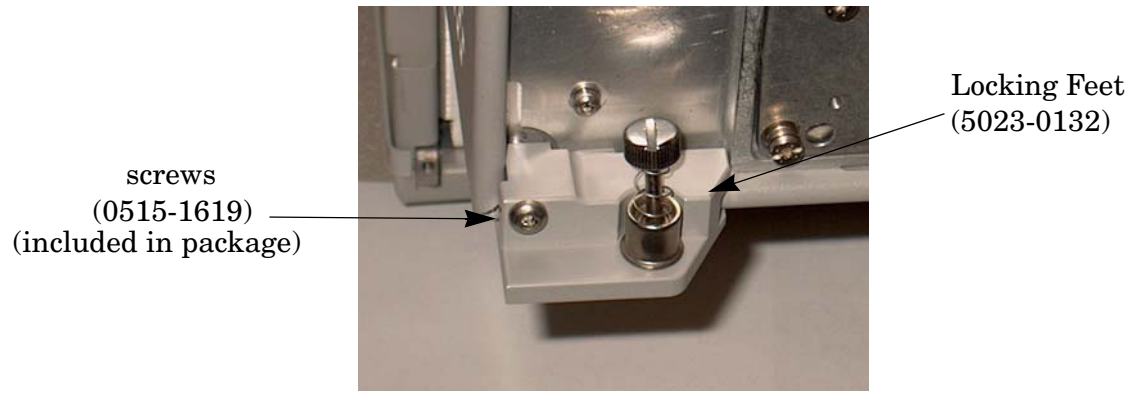
1. Remove the feet from the bottom of the network analyzer. Refer to Figure 5.
2. Remove the 2 lower standoffs and screws (0515-1619) from the rear panel on the network analyzer. Refer to Figure 5.

Figure 5 Bottom Feet



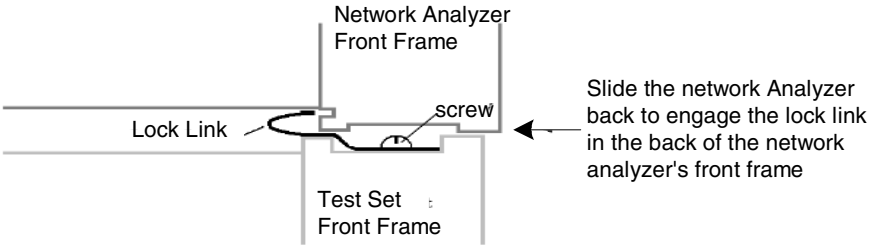
3. Install the two rear locking feet (5023-0132) using the included screws (0515-1619), where the standoffs were removed. Refer to Figure 6.

Figure 6 Installing Lock Feet



4. Place the network analyzer on top of the Test Set and ensure that the front frame of the network analyzer is positioned slightly forward of the locks that are attached to the Test Set. Slide the network analyzer back so the locks engage the front frame of the analyzer. Refer to Figure 7.

Figure 7 Locking the Analyzer's



5. Secure the network analyzer's lower locking feet to the Test Set upper locking feet, using the spring–loaded screws on the locking feet. Refer to Figure 8. If the network analyzer's lower locking feet are not aligned with the screw holes in the Test Set's upper locking feet, loosen the screws securing the feet to the instrument slightly to align.

Figure 8 Locking Feet Screws

NOTE There are two Lock-Feet kits available. Refer to "Contacting Agilent Sales and Service Offices" on page 59 for ordering information.

- PNA – 5023-0132 (Kit includes locking feet and screws)
- Test Set – 5063-9253 (Kit includes lock links, locking feet and screws)

RF Cable Connections

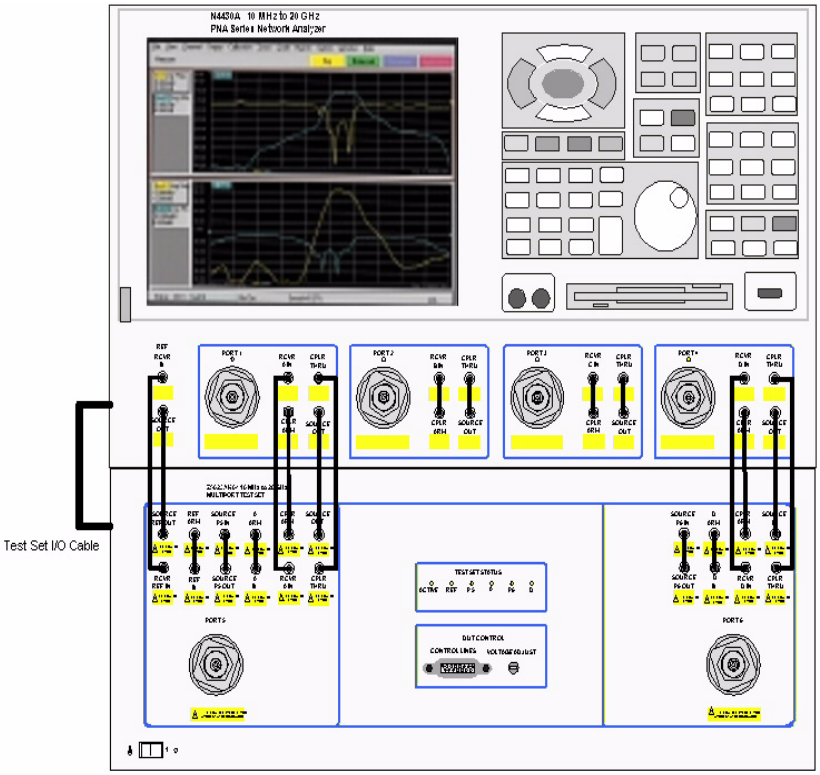
Figure 9 on page 17 shows the setup configuration of the Z5623AK64 High Power Test Set and how it should be configured to the N5230A 4-Port PNA-L Series Network Analyzer.

1. Connect the cables as listed in Table 7.

Table 7 Cable Connection

RF Cables	From (PNA)	To (Test Set)
Z5623-20418	Port Reference SOURCE OUT	SOURCE REF OUT
Z5623-20418	Port 1 CPLR ARM	CPLR ARM
Z5623-20418	Port 1 SOURCE OUT	SOURCE OUT
Z5623-20418	Port 4 CPLR ARM	CPLR ARM
Z5623-20418	Port 4 SOURCE OUT	SOURCE OUT
Z5623-20419	Port Reference RCVR IN	RCVR REF IN
Z5623-20419	Port 1 RCVR A IN	RCVR A IN
Z5623-20419	Port 1 CPLR THRU	CPLR THRU
Z5623-20419	Port 4 RCVR D IN	RCVR D IN
Z5623-20419	Port 4 CPLR THRU	CPLR THRU

Figure 9 Z5623AK64 Setup Configuration

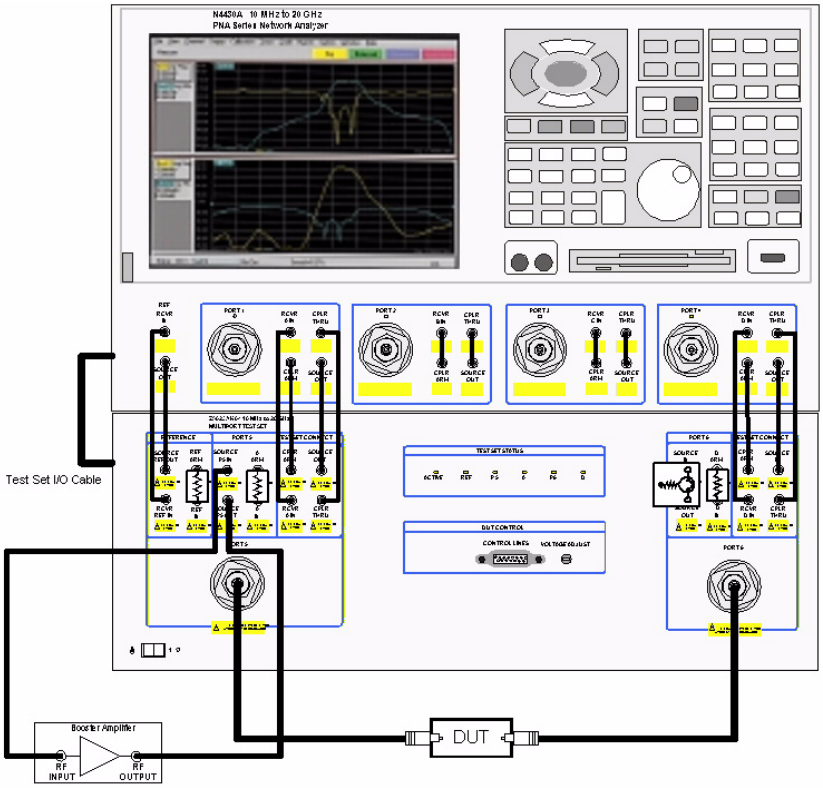


2. Connect Test Set I/O cable (8120-6818), supplied, between the PNA-L and the Z5623AK64 Test Set Interconnect on the rear panel. Do not connect this to the Z5623AK64 Pass Thru Interconnect.

High Power System Setup

CAUTION A high power isolator or attenuator MUST be inserted at the P6 SOURCE OUT and SOURCE IN front panel connectors to protect the internal test set switch and PNA solid-state transfer switch. 20 dB of minimum isolation is recommended. Optimum power level to all PNA receivers is –15 dBm. Insert the attenuators to the receivers (A, D and REF) to reduce power accordingly. Set the initial instrument state to –65 dBm test port power level to reduce risk of damage when turning on the unit.

Figure 10 High Power Forward Direction



DUT Control

Setting the Control Line

This section describes the electrical characteristics of the control line, connection to a DUT and an external dc power supply. For more information regarding the control lines refer to Table 12 on page 32.

Pin Assignment

Figure 11 Pin Assignment for the Control Line

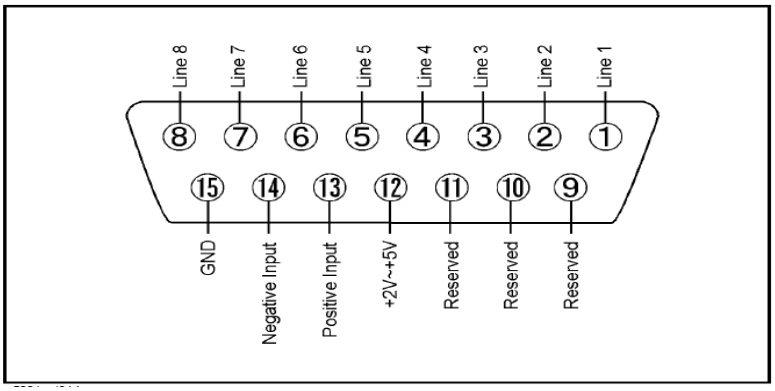


Table 8 Pin Assignment

Pin Number	Signal Name	Description
1	Line 1	output port of line 1
2	Line 2	output port of line 2
3	Line 3	output port of line 3
4	Line 4	output port of line 4
5	Line 5	output port of line 5
6	Line 6	output port of line 6
7	Line 7	output port of line 7
8	Line 8	output port of line 8
9		not used
10		not used
11		not used
12	+2 V to +5 V	The voltage input to pin 13. (The voltage can be varied by rotating the voltage adjustment trimmer on the front panel).
13	Positive Input	Input a signal that is outputted when each line is high from the pin 12 or external dc power supply.
14	Negative Input	Input a signal that is outputted when each line is low from the external dc power supply. Able to output 0 V as low from the each line by connecting to pin 15.
15	Gnd	ground terminal

Figure 12 Block Diagram of DUT Control

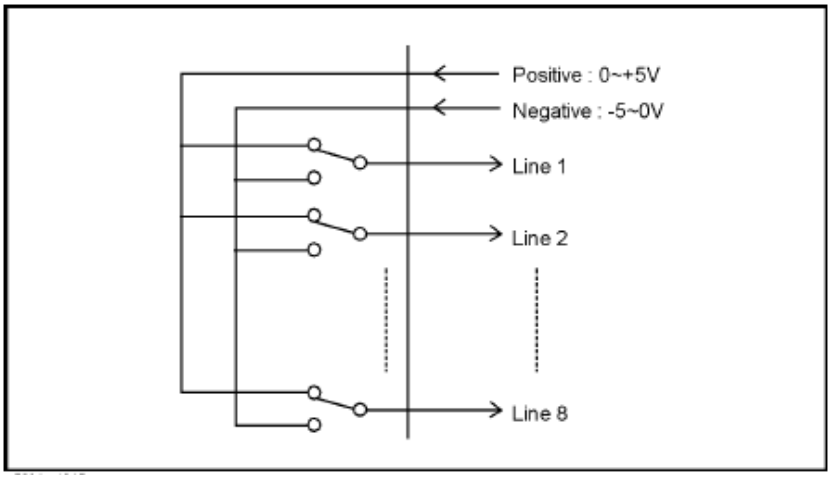


Table 9 Specifications

Item	Specifications
Connector Shape	10-pin female D-Sub
Voltage Range:	
Positive Input	0 to +5 V
Negative Input	–5 to 0 V
Maximum Current	100 mA (in total of each line)
Impedance	< 10 Ω
Range of Variable Voltage	+2 to +5 V

Setting the Voltage of the Variable Voltage Output

The output voltage of pin 12 can be varied from +2 to +5 V. Perform the following procedure to set the voltage:

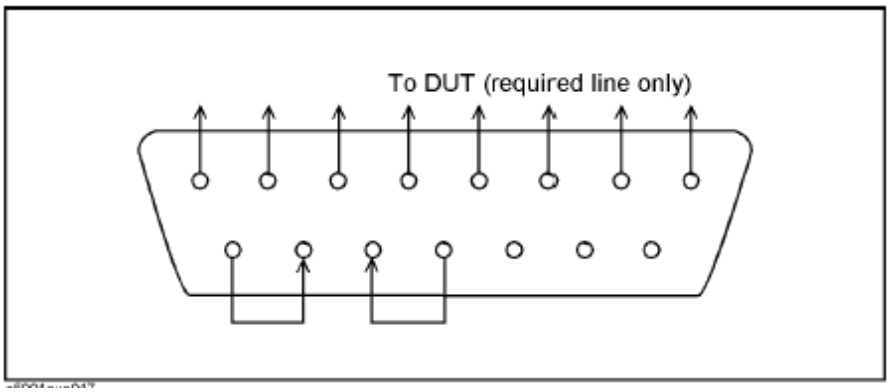
1. Turn On Z5623AK64.
2. Measure the voltage between pin 12 and 15 using a multimeter.
3. Rotate the voltage adjustment trimmer on the front panel until the multimeter indicates the appropriate voltage.

Connect to the DUT

Figure 13 shows an example of the connection between the DUT and the Z5623AK64 *without* an external dc power supply. Input the signals from pin 12 and 15 to the Positive Input and Negative Input respectively and connect each line to the control terminal of the DUT.

CAUTION The path that can be shorted is between pin 12-13 and the pin 14-15 only. Damage may result if any other path is short-circuited.

Figure 13 Connecting to the DUT



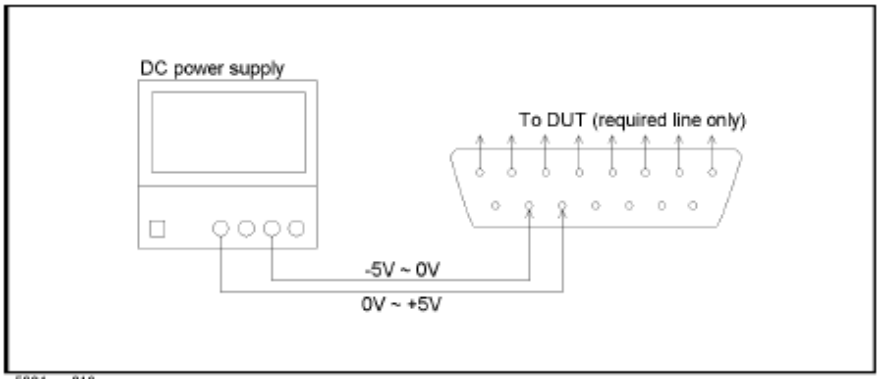
Connecting to the DUT With an External dc Power Supply

Figure 14 shows an example of the connection between the DUT and the Z5623AK64 with an external dc power supply. Input the High and Low signals from the external power supply to the Positive Input and Negative Input respectively, and connect each line to the control terminal of the DUT.

CAUTION Perform the procedure "Turning On the Z5623AK64 → Connecting the DUT → Turning on the external power supply". Reverse the procedure to turn Off the Z5623K64. The Z5623AK64 may break down if a dc current is passed through it when it is turned Off.

CAUTION Do not short-circuit between the pins, it may cause damage.

Figure 14 Z5623AK64 to the DUT and External Power Supply



Controlling the Test Set

The Z5623AK64 High Power Test Set is considered a “slave” instrument. The PNA-L must used to control the Test Set. There are three methods to control the Test Set. Methods 1 and 2 will be explained in this manual. Refer to the standard PNA manual for the third method.

- The PNA Interface Control.
- The PNA GPIB Command Processor.
- External Test Set I/O connector through SCPI and COM programming commands. Refer to the standard PNA manual.

Key Conventions

The following key conventions are used throughout this document.

- **[HARDKEYS]** are labeled front panel keys
- **SOFTKEYS** are unlabeled keys whose function is indicated on the instrument display

PNA Interface Control

The Interface Control feature allows remote commands and data to be send to the following PNA rear-panel Interfaces: GPIB, Material Handler I/O, Test Set I/O, and Auxiliary I/O.

This section includes only the features required in the Interface Control for the Z5623AK64 High Power Test Set. Applications and feature information, such as those listed below, can be found in the PNA’s Help Menu listed under “Interface Control.”

- Overview
- How to Access Interface Control Settings
- Interface Control Dialog Box
- Z5326A H08 Test Set Commands
- Other Connectivity Topics

Overview

The Interface Control feature also allows you to send data to control external Test Set without needing to create a remote program. The PNA manages the timing and required interface setup.

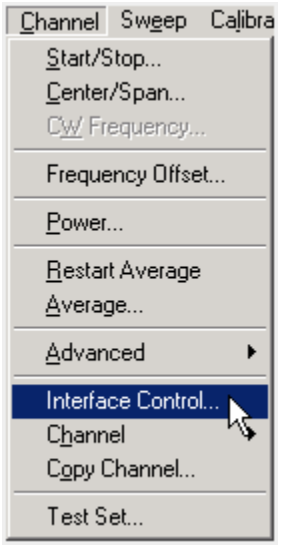
A unique set of control data can be sent for each channel. In addition, a unique set of control data can be sent before the channel sweep starts and after the sweep ends.

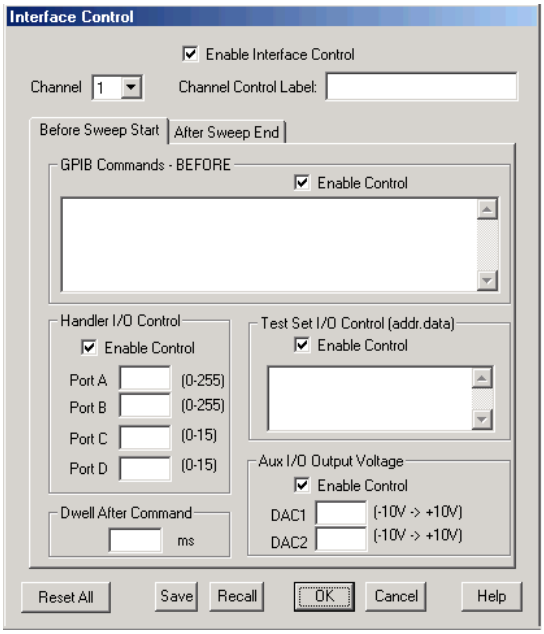
Interface Control settings can be saved and recalled from the Interface Control dialog box or with instrument state **Save** and **Recall**.

Control data can only be WRITTEN to the interfaces, NOT READ from the interfaces.

Control data is sent in the following order and *cannot* be changed.

1. GPIB Interface
2. Material Handler Interface
3. Test Set Interface
4. Aux Interface
5. Dwell Time





An instrument **Preset** will reset all of the fields to their default settings.

NOTE If an error is encountered when sending Interface Control data, an error message is displayed on the PNA screen. The Channel Trigger State is set to Hold. You must fix the condition that caused the error, then change the Channel Trigger State to its original setting.

Enable Interface Control:

Enables and disables ALL Interface Control communication. When cleared (default setting) Interface Control is disabled and NO data is sent. To send data, the individual interfaces must also be enabled.

Channel:

Specifies the channel number for dialog settings. Each channel is configured individually. The list box shows the channels that currently have measurements. There must be at least one measurement present in order to make the settings.

Channel Label:

Specifies the label to be displayed on the PNA screen during the channel sweep.

Before Sweep Start - After Sweep End Tabs.

NOTE While using Interface Control, the PNA must be in GPIB System Controller mode. Once this is complete you must restart the PNA application to go back to Talker/Listener.

Commands /data for all four interfaces can be sent both Before Sweep Start and After Sweep End. However, they are configured and enabled on separate tabs of the Interface Control dialog box. For example, to send GPIB commands both Before and After a PNA sweep, the Enable Control check box must be selected and commands entered on BOTH the Before Sweep Start and After Sweep End tabs.

Before Sweep Start:

The data is sent BEFORE the first trace on the channel begins sweeping.

After Sweep End:

The data is sent AFTER the last trace on the channel completes sweeping.

Test Set I/O

Enable Control:

Enables and disables sending data out of the External Test Set I/O connector.

Multi-line Edit Control:

Each line contains a Write command using the following syntax:

address: any positive integer

value: any positive integer

Address and value are separated by a period, for example:

0.2
16.127

Entries should be separated by a new line or carriage return. The PNA front-panel **[Enter]** key inserts a new line into the field. All entries are sent out the External Test Set I/O using the WriteData Method. The number of entries is limited only by the available memory of the PNA.

Dwell After Command:

Specifies a wait time, in milliseconds, after all commands to all interfaces are sent. Any positive integer is allowed. This is used to allow all external devices to settle before beginning a measurement. An erratic trace could indicate that more settling time is necessary.

Reset All:

Sets ALL fields on ALL channels to their default values.

Save and Recall

Saves and recalls the contents of the dialog box. If the Interface Control dialog box is populated with settings during an Instrument State Save, the settings are automatically recalled with the instrument state settings. Interface control uses an *.xml file type. An example file is stored on the PNA hard drive. You can recall it into the dialog, or you can open and edit it with a word processor, such as Word Pad.

OK:

Applies the settings and closes the dialog box.

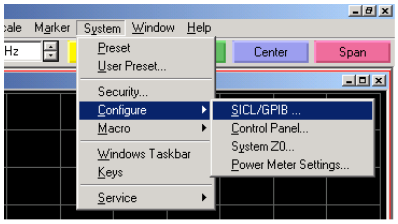
Cancel:

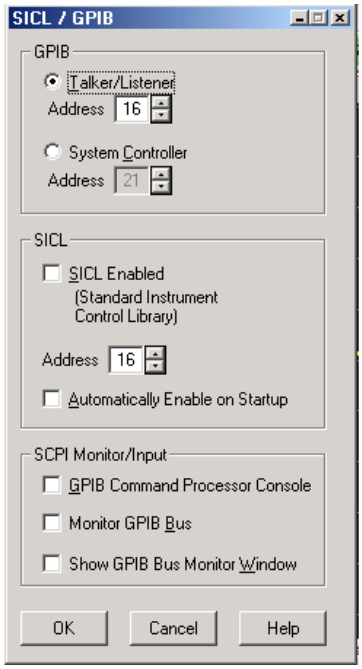
Does not apply changes that were made and closes the dialog box.

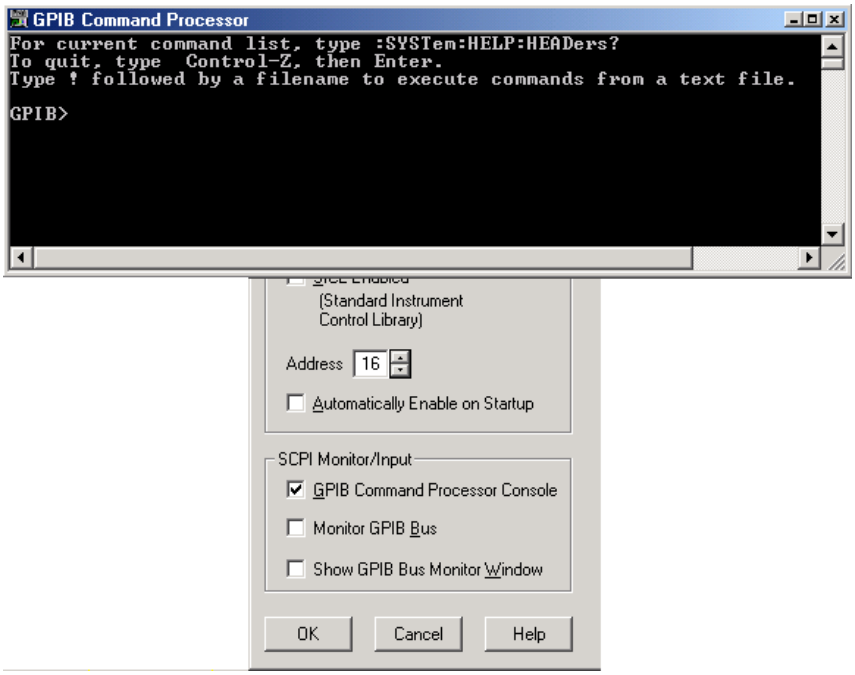
NOTE Z5623AK64 Test Set I/O Commands can be found in Table 10 on page 30. The Address and Data commands can be entered into the Test Set I/O control.

PNA GPIB Command Processor

To control the Z5623AK64 Test Set through the GPIB Command Processor press **[Menu/Dialog]** then tab to **System**, select **Configure** > **SICL/GPIB** and check the GPIB Command Processor Console box.







Write Commands

Once the GPIB Command Processor Console is open, commands can remotely control the external Test Set I/O connector by sending the following:

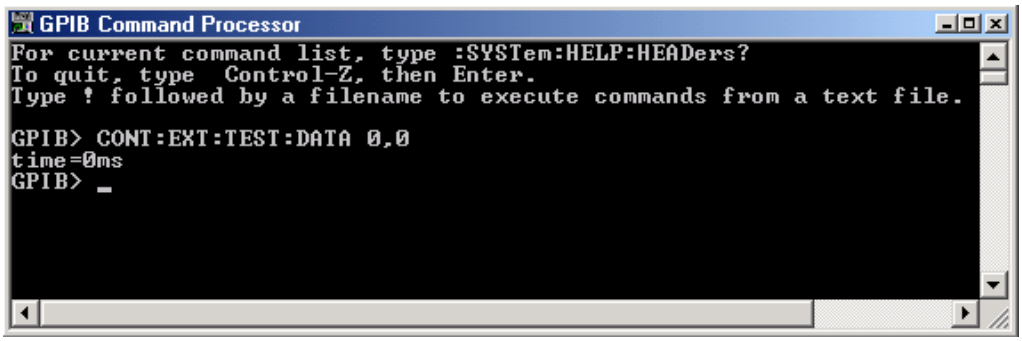
`CONTrol:EXTernal:TESTset:DATa<addr>,<data>`

Parameters:

<addr> Decimal equivalent of the 13 bit binary address

<data> Decimal equivalent of the 13 bit binary data

Example: CONT:EXT:TEST:DATA 0,0



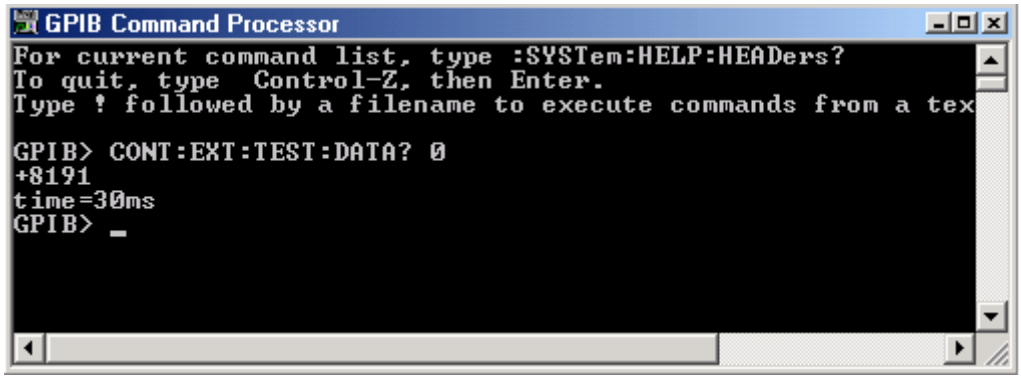
Read Commands

`CONTrol:EXTernal:TESTset:DATa<addr>,<data>`

Parameters:

<addr> Decimal equivalent of the 13 bit binary address

Example: CONT:EXT:TEST:DATA? 0



Reads the decimal equivalent of the binary data from the specified address.

Test Set I/O Interface Commands

Switch Address and Data

Table 10 and Table 11 on page 31 contain the information to set the internal switch paths of the Z5623AK64 Test Set. For more information about the internal switches refer to "Theory of Operation" on page 48.

NOTE All switches must be set with each command sent.

Table 10 Test Set Switch Address and Data

Test Set I/O Address and Data Switch				
Address	**Data (Value)**	**Data AD12-AD0**	**Description**	**Bit Data** 0=internal 1=external
0	0	0000000000000	Sets test set into bypass mode or internal	
0	31	0000000011111	Sets test set into high power mode or external for forward measurements	
0	15	0000000001111	Sets test set into high power mode or external for reverse measurements	
0		00000000xxxxB	Bit 0 controls Port 1 and 5 source switch SW1	0,1
0		00000000xxxBx	Bit 1 controls Port 1 and 5 receiver switch SW2	0,1
		00000000xxBxx	Bit 2 controls Port 4 and 6 source switch SW3	0,1
0		00000000xBxxx	Bit 3 controls Port 4 and 6 receiver switch SW4	0,1
0		00000000Bxxxx	Bit 4 controls reference switch SW5	0,1
x indicates unknown user bit state				
B indicates bit of interest				

There are 32 individual switch combinations for the Z5623AK64. To select a Test Set switch configuration, all 5 switches must be set. To do this you must add AD4 to AD0 binary number and convert this to a decimal equivalent. Refer to Table 11 on page 31.

Table 11 Switch Address and Data Example

Address 0		**Bit Decimal Equivalent**			**16**	**8**	**4**	**2**	**1**
SW Data = 0 to 31					AD4	AD3	AD2	AD1	AD0
Switch					SW5	SW4	SW3	SW2	SW1
0	Add bits AD4 to AD0 = 0				0	0	0	0	0
31	Add bits AD4 to AD0 = 31				1	1	1	1	1
12	Example: SW5, SW2, SW1 internal, SW ELSE external				0	1	1	0	0

Control Lines

Table 12 and Table 13 on page 33 contain the information to set the control lines of the Z5623AK64 Test Set. Refer to "DUT Control" on page 19 for more information.

NOTE All DUT control lines must be set with each command sent. Logic 0 = high.

Table 12 Test Set DUT Control Address and Data

Test Set I/O Address and Data DUT Control Lines				
Address	**Data (Value)**	**Data AD12-AD0**	**Description**	**Bit Data** 0= + internal 1= - external
16	0	0000000000000	All DUT Control Lines set to 0 or + voltage	
16	225	0000001111111	All DUT Control Lines set to 1 or – voltage	
16		00000xxxxxxxB	DUT Control Line 1	0,1
16		00000xxxxxxBx	DUT Control Line 2	0,1
16		00000xxxxxBxx	DUT Control Line 3	0,1
16		00000xxxxBxxx	DUT Control Line 4	0,1
16		00000xxxBxxxx	DUT Control Line 5	0,1
16		00000xxBxxxxx	DUT Control Line 6	0,1
16		00000xBxxxxxx	DUT Control Line 7	0,1
16		00000Bxxxxxxx	DUT Control Line 8	0,1
x indicates unknown user bit state				
B indicates bit of interest				

There are 256 individual DUT control line combinations for the Z5623AK64. To select a Test Set DUT control line configuration, all 8 DUT control lines must be set. To do this you must add AD7 to AD0 binary number and convert this to a decimal equivalent. Refer to Table 13 on page 33.

Table 13 DUT Control Address and Data Example

Address 16									
Bit Decimal Equivalent		**128**	**64**	**32**	**16**	**8**	**4**	**2**	**1**
DUT Data = 0 to 255		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
Control Lines		**Line 8**	**Line 7**	**Line 6**	**Line 5**	**Line 4**	**Line 3**	**Line 2**	**Line 1**
0	Add bits AD7 to AD0 = 0	0	0	0	0	0	0	0	0
255	Add bits AD7 to AD0 = 255	1	1	1	1	1	1	1	1
85	Example: DUT8, DUT6, DUT4, DUT2 + Voltage DUT ELSE – Voltage	0	1	0	1	0	1	0	1

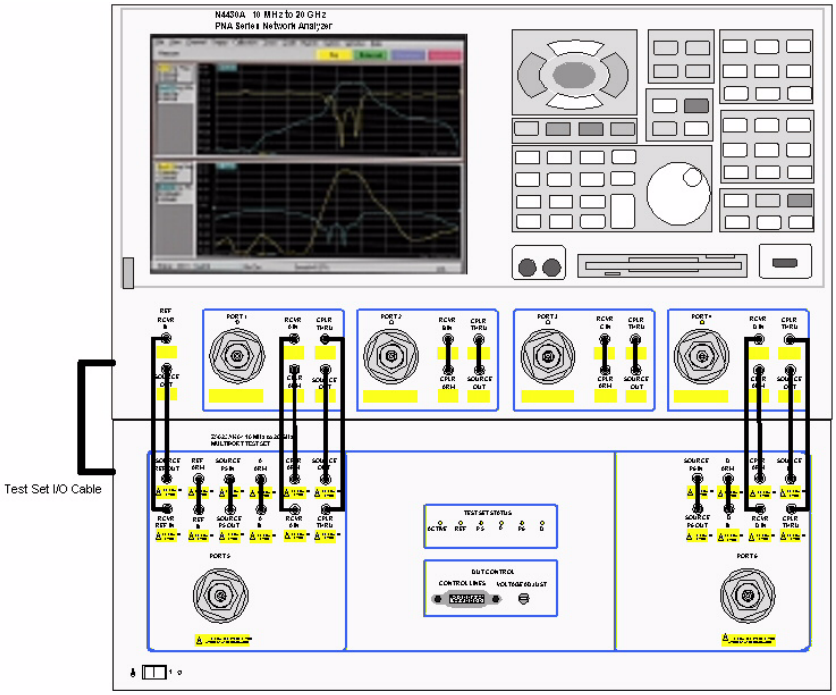
High Power Measurements With Z5623AK64

The Z5623AK64 and N5230A 4-Port PNA-L with Option 245 can be configured to measure high power devices. This ability is useful if the required power for the device under test is greater than what analyzer can provide, or if the maximum output power from the amplifier under test exceeds safe input limits for the analyzer. This section describes how to set up the analyzer and test set to perform high power measurements.

Initial Setup

1. Connect the Test Set to the PNA. See Figure 15. All equipment should be turn off at this time. Connect the jumpers between the Test Set and the PNA for both 1 and 5, 4 and 6 and the Reference Access ports.

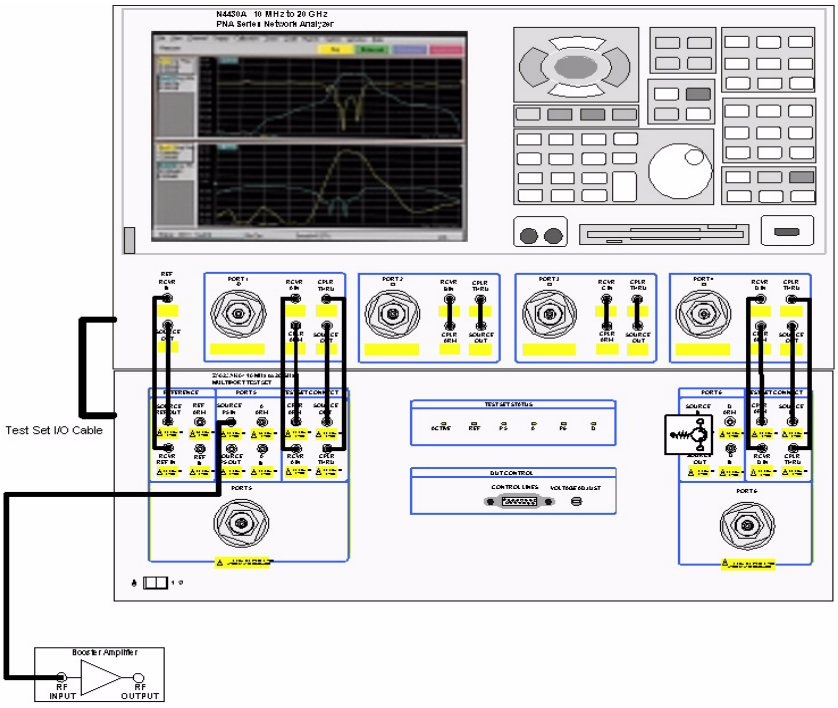
Figure 15 Setup Configuration



2. Remove the jumpers on the front panel of the Test Set if the Z5623AK64 is in the shipped mode configuration (all the jumpers are still on).
3. Connect the booster amplifiers RF Input connector to the SOURCE P5 IN access connector on the front panel of the Z5623AK64. Ensure that the amplifier is turned Off at this time.

4. Place an isolator or attenuator between the SOURCE P6 IN and SOURCE P6 OUT on the port 2 side. The isolators placement is important to ensure that the signal is attenuated into SOURCE P6 IN. The reverse attenuation or isolation factor of the isolator should be 20 dB or greater.

Figure 16 Connect Booster Amplifier



Determining Power Levels

Before continuing, save this state and set it up as the **User Preset**. The User Preset Conditions can be found in the PNA Series Network Analyzer Help System.
Press **[Menu/Dialog]** then tab to **Help > Network Analyzer Help**. Type in **User Preset**. The final state can then be re-saved as the User Preset to avoid an over power condition from the factory preset. To find the User Preset press **[Menu/Dialog]** then tab to **System**, select **User Preset** and check **User Preset Enable**. Click **Save current state as User Preset** > **OK**.

5. Turn On the analyzer and Test Set and reduce the power level to –20 dBm by pressing **[Menu/Dialog]** then tab to **Channel** and select **Power.** Enter **[–20]** in the Test Port Power entry area. Port Power Coupled should be checked to ensure that ports 1 and 2 power levels are the same. Un-Couple ports should be used when adjusting the S12 power level to a different power level from Port 1.
6. Set the Z5623AK64 Test Set so the external booster amplifier is in the RF path. See Test Set I/O Interface Commands Table 10 on page 30 and Table 11 on page 31 to set the Test Set switches to external. This will place the booster amplifier in the RF path.
7. Turn On the booster amplifier.
8. Using a high power meter and sensor, measure the output power from the booster amplifier RF Output.

NOTE Additional attenuation may have to be added between the coupler and the power meter depending on the power used.

---

9. Verify the gain of the booster amplifier(s). For example; if the analyzer output power level was set to –20 dBm and the output power measured from the open end of the coupler was –5 dBm, the gain of the booster amplifier would be +15 dB.
10. Verify that the power measured in the previous step is within the acceptable limits (less than +43 dBm for the SOURCE P5 OUT port).
11. Turn Off the booster amplifier.
12. Estimate the maximum power level that will be needed to force the DUT into compression. Acceptable limits are less than +43 dBm for the SOURCE P5 OUT port.

CAUTION Do not command the Test Set to engage or disengage the amplifier from the Port 1 RF path while the amplifier is on. This can damage the internal RF switches in the Test Set.

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13. Connect the booster amplifier RF OUTPUT connector to the SOURCE P5 OUT connector on the front panel of the Z5623AK64. Ensure that the amplifier is turned Off at this time.
14. Turn On the booster amplifier.

15. Measure the output power from the Test Set's REF ARM port, using a high power meter and sensor.
16. Turn Off the booster amplifier.
17. Measure the output power from the Test Set's A ARM port, using a high power meter and sensor.
18. Turn Off the booster amplifier.
19. Estimate the maximum power level that will be needed to force the DUT into compression.

Selecting Power Ranges and Attenuator Settings

20. Select a PNA power range that will not exceed the maximum estimated power level, but will force the DUT into compression. For example; if your booster amplifier has a gain of +15 dB and the DUT will compress if supplied with +15 dBm, then adjust the analyzer's output power not to exceed +0 dBm. Select **[Menu/Dialog]** then tab to **Channel**, select **Power >** uncheck **Auto** and enter **[10]** into the entry area. The Port Power Coupled can be verified to ensure that Port 1 and 2 power levels are the same, or uncoupled if Port 1 and 2 power level requirement are different.
21. Estimate the maximum amount of gain that could be provided by the DUT and as a result, the maximum amount of power that could be received by Test Port 6 when the DUT is in compression. For example; if a DUT with a maximum gain of +10 dB receives an input of +10 dBm, the maximum amount of power that could be received by Test Port 6 is +20 dBm. An isolator or attenuator may be required depending on the amount of power at Test Port 6. An isolator can be placed between the Test Set's SOURCE P6 OUT and SOURCE P6 IN to protect the Test Set and the PNA. The isolators placement is important to ensure that the signal is attenuated looking into SOURCE P6 IN. The reverse attenuation or isolation factor of the isolator should be 20 dB or greater.
22. Calculate the amount of attenuation needed so that the optimum PNA receiver power level of –15 dBm is not exceeded. Refer to your PNA specifications to optimize power levels to the receiver ports.

In following example it will be necessary to take the following into consideration:

- Measured at the Test Set's REF ARM = –2 dBm.
- Estimated compression power = –2 dBm
- The optimum PNA receiver power level is –15 dBm.
- Loss thru the REF switch and cables in the Test Set is approximately 3 dB.

With the previous points in mind, the amount of attenuation can be calculated from the following equations:

- Attenuator REF ARM setting = –2 dBm – (–15 dBm) – (–3 dB) = 10 dB
- REF ARM attenuator value = 10 dB

23. Place the attenuator(s) on Test Set's REF ARM to the value calculated in step 22.
24. Turn On the booster amplifier.
25. Measure the output power from the Test Set's REF ARM, using a high power meter and sensor.
26. Verify that the power measured in the previous step is within the acceptable limits (–12 dBm the RCVR REF IN).
27. Calculate the amount of attenuation needed so that the optimum PNA receiver power level of –15 dBm is not exceeded. Refer to your PNA specifications to optimize power levels to the receiver ports.

In the following example it will be necessary to take the following into consideration:

- Measured at the Test Set's A ARM = –2 dBm.
- Estimated compression power = –2 dB.
- The optimum PNA receiver power level is –15 dBm.
- Loss thru the A switch and cables in the Test Set is approximately 3 dB.

With the previous points kept in mind, the amount of attenuation can be calculated from the following equations:

- Attenuator A ARM setting = –2 dBm – (–15 dBm) – (–3 dB) = 10 dB
- A ARM attenuator value = 10 dB

28. Place the attenuator (s) on Test Set's A ARM to the value calculated in step 27.
29. Turn On the booster amplifier.
30. Measure the output power from the Test Set's A ARM, using a high power meter and sensor.
31. Verify that the power measured in the previous step is within the acceptable limits (–12 dBm to A IN).
32. Calculate the amount of attenuation needed between the D ARM and D IN coupler and receivers not exceed the optimum receiver power level of –15 dBm.

In this example, it will be necessary to take the following into consideration:

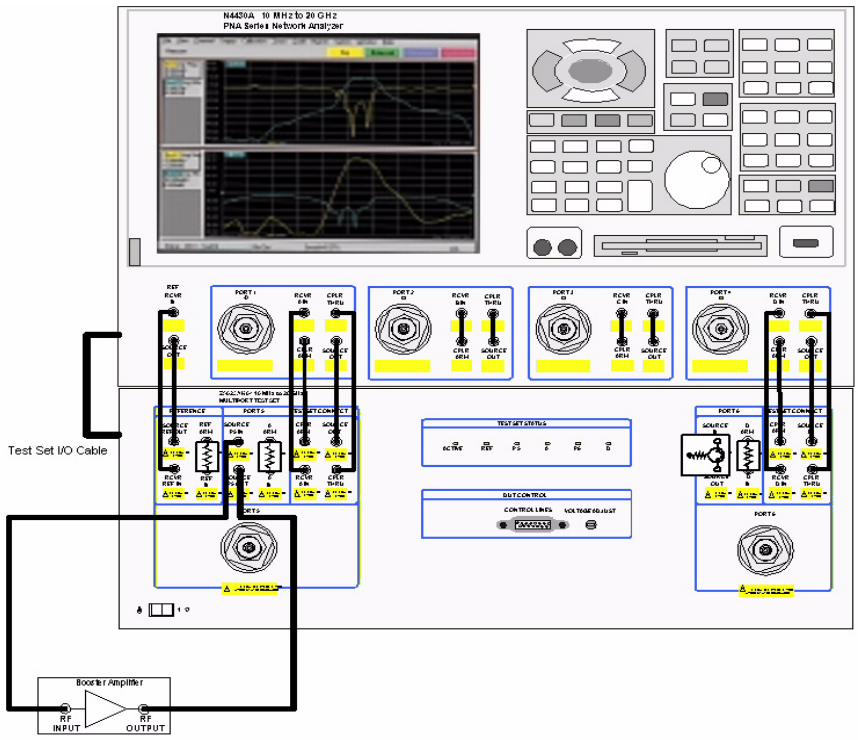
- Power to Test Port 6 is 40 dBm.
- D ARM will be coupled from Test Port 6.
- The coupling factor of Test Port 6 is 13 dB.
- The optimum receiver power level is –15 dBm.
- Loss thru the D RCVR switch and cables in the Test Set is approximately 3 dB

With the previous points kept in mind, the amount of attenuation can be calculated from the following equations:

- Attenuator D ARM setting = +40 dBm – 13 dB – (–15 dBm) (–3 dB) = 45 dB
- D ARM attenuator value = 45 dB

33. Place the attenuator (s) on Test Set's D ARM to the value calculated in step 32.

Figure 17 Booster Amplifier, Attenuators and Isolator Placement



34. Turn On the booster amplifier.

CAUTION Do *not* press Preset unless you have turned Off the booster amplifier(s) or have saved this state and renamed it to User Preset. Pressing Preset will return the analyzer to its default power level and default internal attenuator settings. The increase in power may result in damage to the DUT or analyzer.

---

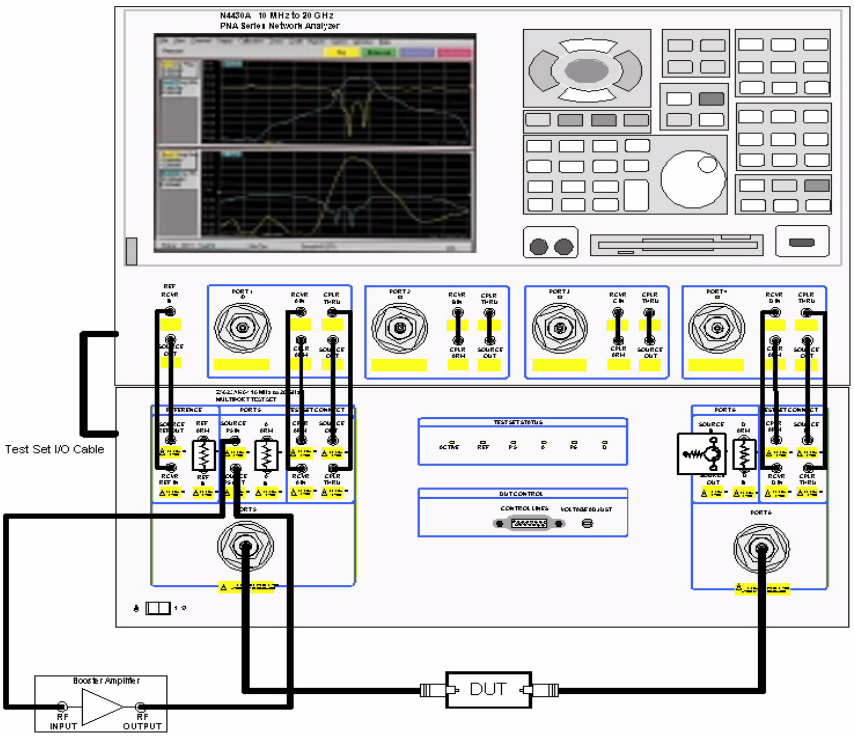
35. Measure the output power from test Port 1 using a high power meter and verify that it is as expected.
36. High power isolators should be inserted between the SOURCE OUT and CPLR IN front panel ports on the Test Set if you are measuring a highly reflective device.

Final Setup

37. Confirm that all power and attenuator settings are correct and set the following measurement: Press **[Menu/Dialog]** then tab to **Trace**, select **Measure** > **S21**.
38. Perform a response calibration:
    - Connect the test port cables to form a thru configuration.
    - Press **[Menu/Dialog]** then tab to **Calibration**, select **Calibration Wizard** > **Unguided Calibration Use Mechanical Standards** > **Next** > **THRU Response** > **Next**. Follow analyzers window prompts to finish calibration.

39. Make the connection as shown in Figure 18. Turn on the DUT and measure the S21 gain of the amplifier under test to confirm the proper operation of the measurement test setup.

Figure 18 Connect the DUT



40. Make any other desired high power measurements.

- Ratio measurements, such as gain, will be correctly displayed. However, the displayed absolute power levels on the analyzer will *not* be correct. To correctly interpret power levels, gain of the booster amplifier and attenuator values must be taken into consideration.

NOTE At this time a Full 2 or 4 port calibration cannot be performed in the High Power mode. To perform a Full 2 or 4 port calibration the PNA must have N-port firmware to control the reference channel of the Test Set.

If no calibration has been performed or if the instrument is in an un-calibrated state, the following must be taken into consideration when interpreting the measured data:

- The value of attenuation added to receiver A and D.
- The R channel reference level supplied from the Test Set.
- Protection of the internal parts for the Test Set and PNA.

Test Set Internal Configurations

The Z5623AK64 can be internally configured to allow different application requirements. This section describe the Test Set's internal configurations.

There are two basic mode configurations.

- Bypass
- High Power

Bypass

The bypass mode sets the Test Set's internal switches so that the source, receiver and reference are all directed to the PNA. Figure 19 shows each switch path. Each switch has been set so information received from the PNA is directed back to the PNA. All 4 ports of the PNA are operational. Figure 20 on page 43 shows the paths of the PNA and Test Set.

Figure 19 Bypass

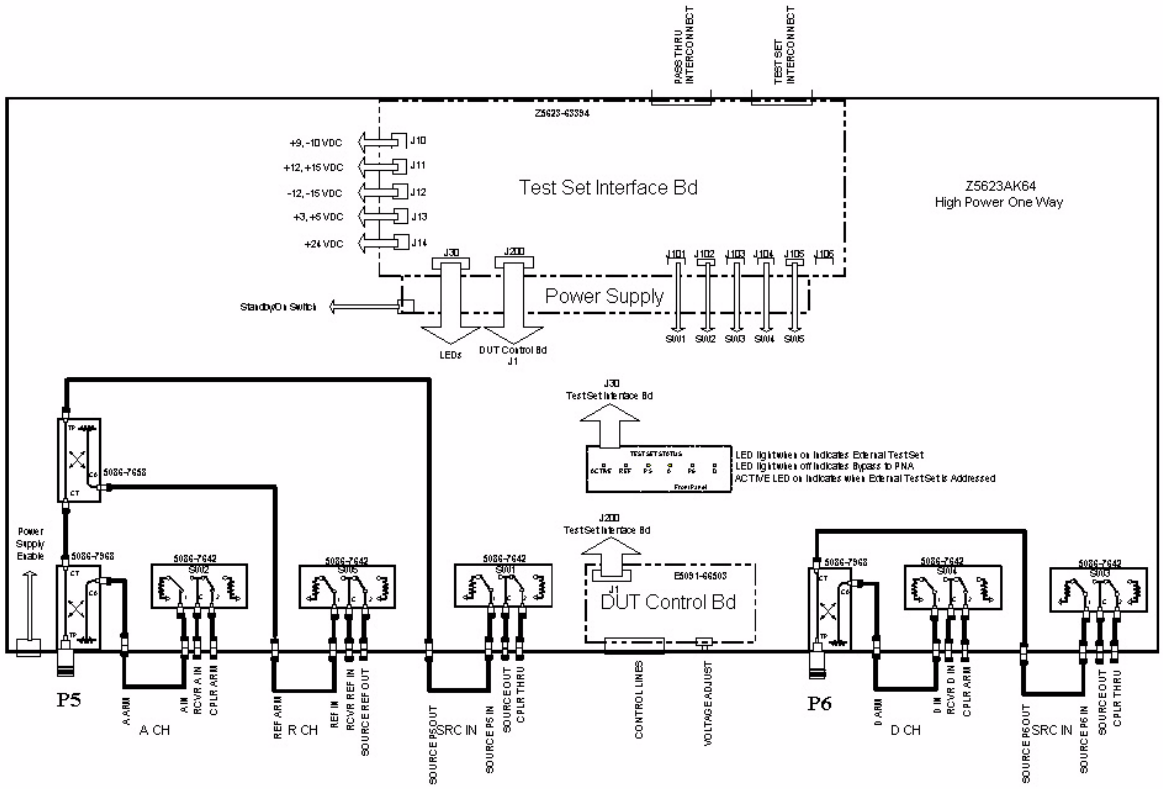
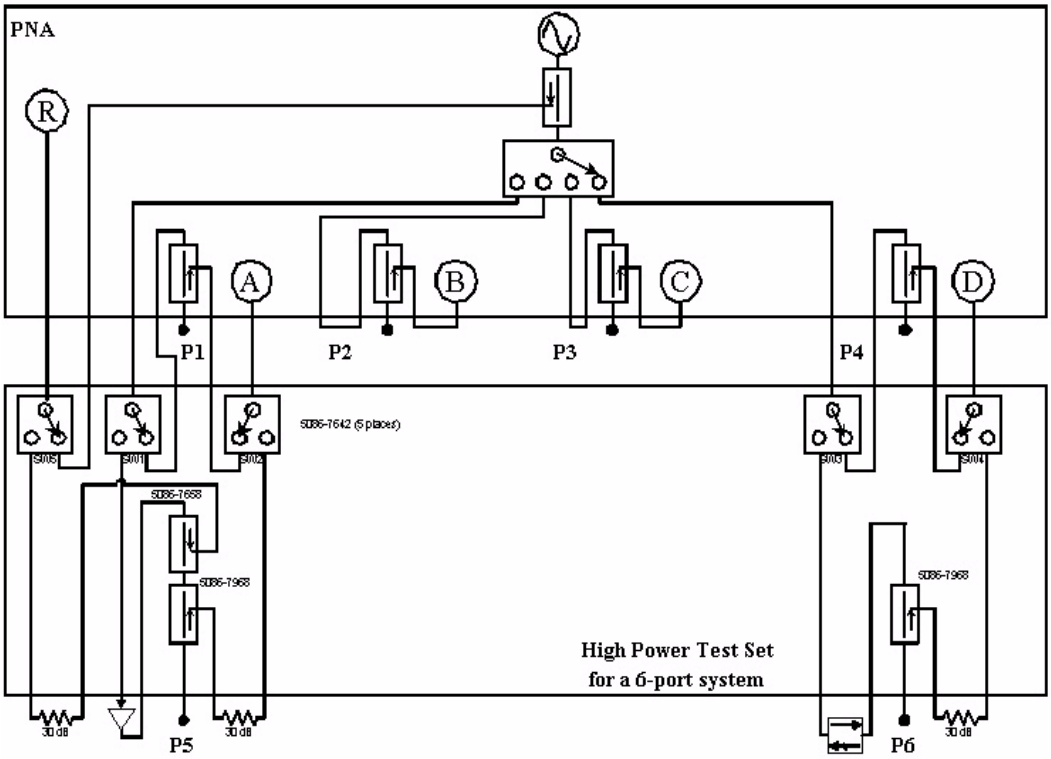


Figure 20 PNA and Test Set in Bypass



High Power

The high power mode sets the Test Set's internal switches so that the source, receiver and reference are all directed to the Test Set. Ports 1 and 4 of the PNA are non operational in this configuration. Each switch shown in Figure 21 are now engaged for the high power forward measurements. Figure 22 on page 45 shows the paths of the PNA and Test Set.

Figure 21 High Power

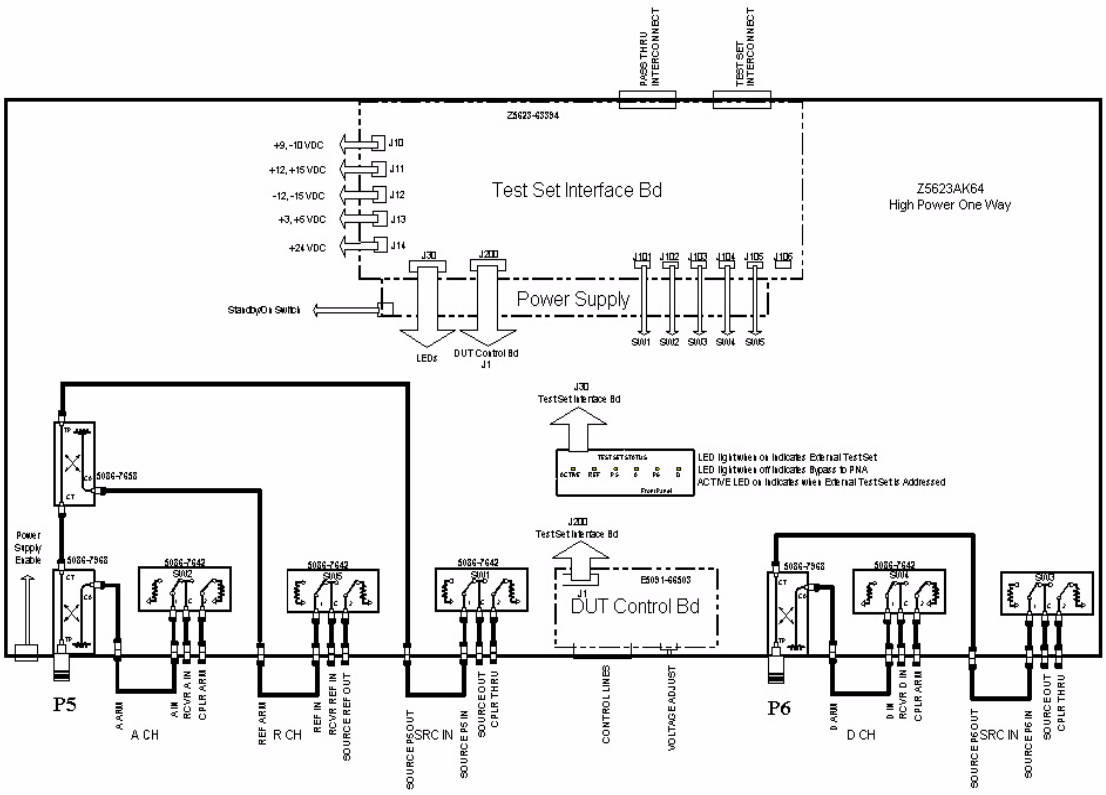
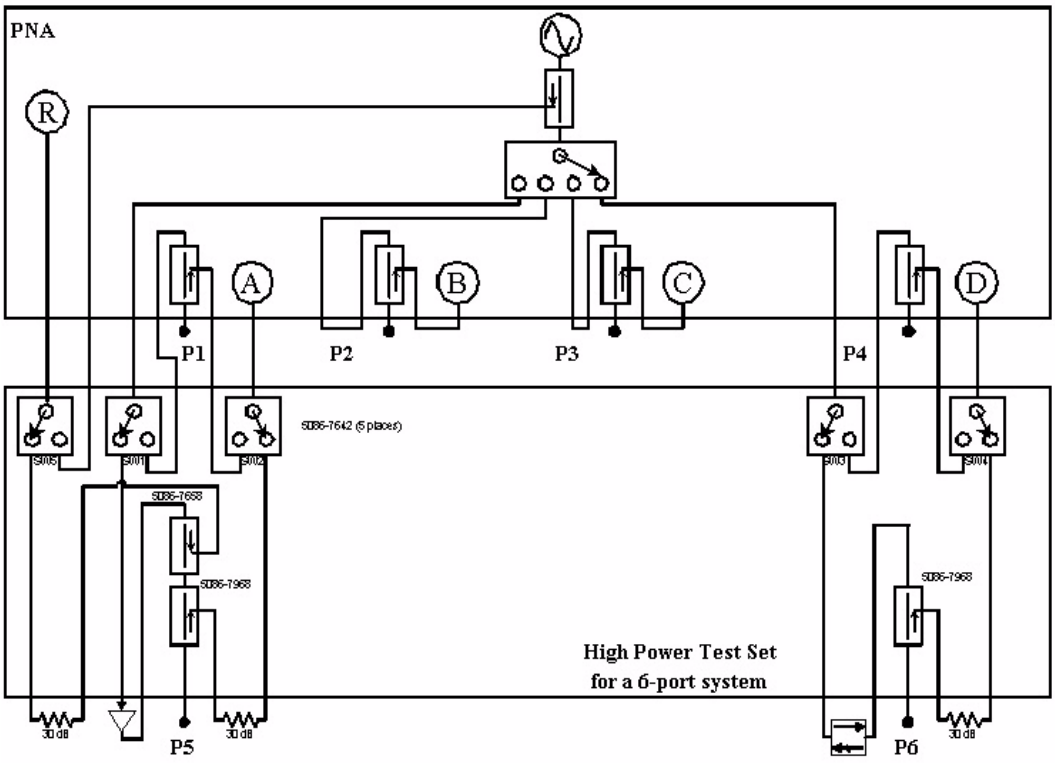


Figure 22 PNA and Test Set High Power



Specification

Specifications for the Z5623AK64 High Power Test Set are nominal. System performance for the PNA and Test Set are not provided. A functional certificate is only offered for the Z5623AK64.

NOTE Nominal specifications are based on 1 to 2 unit's performance.

NOTE This Test Set, when connected to a PNA, will degrade the performance of the test ports that the Test Set interconnects to. The internal solid-state switch paths reduce Test Port power and power to the receiver ports. This affects not only the test port power of the PNA and also reduces dynamic range. Test Port power of the PNA will be reduced as much as 10 dB and power to the receivers will be reduced by as much as 10 dB. This will decrease the dynamic range by 20 dB.

Declaration of Conformity

For a copy of the manufacturer's Declaration of Conformity for this apparatus, contact your local Agilent Technologies office or sales representative on Page 59.

Servicing the Z5623AK64 High Power Test Set

Service Information

Return to Agilent Technologies factory for servicing or repair. Refer to "Contacting Agilent Sales and Service Offices" on page 59.

WARNING	**No operator serviceable parts inside. Refer servicing to qualified personnel. To prevent electrical shock do not remove covers.**

WARNING	**These servicing instructions are for use by qualified personnel only. To avoid electrical shock, do not perform any servicing unless you are qualified to do so.**

Shipping Instructions

You must always call the Agilent Technologies Instrument Support Center to initiate service before retuning your instrument to a service office. See "Contacting Agilent Sales and Service Offices" on page 59. Always transport or ship the instrument using the original packaging if possible. If not, comparable packaging must be used. Attach a complete description of the failure symptoms.

Theory of Operation

RF Components

SW1 through SW5

SW1 through SW5 are all solid-state switches. Frequency range is 45 MHz to 20GHz.

SW1-Source to 1 and 5

SW1 of the Test Set directs the port 1 Source Out RF signal from the PNA by means of a jumper cable from the PNA port 1 and Test Set port SOURCE OUT access ports. When the Test Set is in the Bypass or Internal mode, SW1 directs the Source Out from the PNA to the Test Set CPLR THRU access port. The Test Set CPLR THRU access port is jumper cabled back to the PNA Port 1 CPLR THRU access port and provides the source output to Port 1 of the PNA. When the Test Set is in the high power or external mode, SW1 directs the Source Out to the Test Set's reference and test Port 5 couplers. This provides the source output for Port 5 of the Test Set.

SW2-Receiver A

SW2 directs the A Receiver signal from the PNA by means of a jumper cable from the PNA and Test Set RCVR A IN access ports. When the Test Set is in the Bypass or Internal mode, SW2 directs the A Receiver signal path from the PNA to the Test Set's CPLR ARM access port. The Test Set CPLR ARM access port is jumper cabled back to the PNA Port 1 CPLR ARM access port and provides the signal path from the PNA test Port 1 coupled arm. When the Test Set is in the high power or external mode, SW2 directs the A Receiver to the Test Set. This provides the signal path from the test Port 5 Coupled Arm.

SW3-Source to 4 and 6

SW3 of the Test Set directs the Port 4 Source Out RF signal from the PNA by means of a jumper cable from the PNA Port 4 and Test Set port SOURCE OUT access ports. When the Test Set is in the Bypass or Internal mode, SW3 directs the Source Out from the PNA to the Test Set CPLR THRU access port. The Test Set CPLR THRU access port is jumper cabled back to the PNA Port 4 CPLR THRU access port, and provides the source output to Port 4 of the PNA.When the Test Set is in the high power or external mode, SW3 directs the Source Out to the Test Set's reference and test Port 6 couplers. This provides the source output for Port 6 of the Test Set.

SW4-Receiver D

SW4 directs the D Receiver signal path from the PNA by means of a jumper cable from the PNA and Test Set RCVR D IN access ports. When the Test Set is in the Bypass or Internal mode, SW4 directs the D Receiver signal path from the PNA to the Test Set's CPLR ARM access port. The Test Set CPLR ARM access port is jumper cabled back to the PNA Port 4 CPLR ARM access port and provides the signal path from the PNA test Port 4 Coupled Arm. When the Test Set is in the high power or external mode, SW4 directs the D Receiver to the Test Set. This provides the signal path from test Port 6 Coupled Arm.

Reference Coupler

The reference coupler provides the REF channel a signal when the Test Set is in high power mode. This removes the effects the amplifier may induce on the signal such as drift and gain. This reference is only provided in the forward direction only P5 => P6. It can also be used making measurements from P5 to Port 2, 3 and 4 on the PNA. When the PNA is in the reverse measurement parameter capability the PNA internal REF must be used and the Test Set SW5 must be set to Bypass the Reference Coupler.

Test Port Couplers P5 and P6

The test port couplers are 3.5 mm male. The couplers can handle up to 40 watts of power to the test and coupler thru ports up to 20 GHz. These ports are use to measure the DUT for high power.

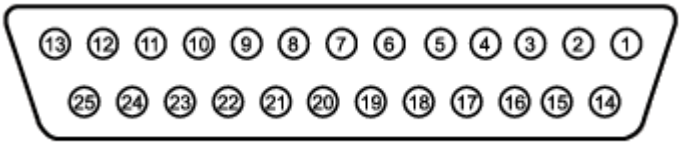
Test Set Interface Control

Refer to the Test Set Interface Schematic while reading the following descriptions:

The Test Set I/O Interface board has Six sections. The first section is the Test Set Interface BD input. This section handles the Addressing, Data and Read/Write TTL instructions from the PNA Test Set I/O. A DB-25 female connector (J1 on the Test Set I/O Interface board) is located on the rear panel of the Test Set and receives external control commands from the PNA. All inputs are ESD protected by CR4 and CR5 on the Test Set Interface BD.

The PNA provides the appropriate timing signals needed for strobing the address and data lines. Below shows the Test Set Interface connector for the Z5623AK64. Pin numbers and locations are shown with a description of the pins used to control the Test Set.

Figure 23 Test Set I/O Interface (J1)



Address/Data I/O Pin Numbers 3, 4, 5, 6, 9, 10, 11, 17, 19, 20, 21, 22 and 23	Address and latched data
Test Set Select Bit SEL0, SEL1, SEL2, and SEL3 Pin Numbers 1, 15, 16, 18	Test Set select bits; tied to ground from the PNA.
LAS Pin Number 8	TTL output - active low address strobe
LDS Pin Number 24	TTL output - active low data strobe
RLW Pin Number 25	TTL output - high-read, low-write

The high power Test Set is activated when the PNA sends a write command with the correct address. The address tells the Interface BD if the Test Set is being activated and which control section of the Interface BD to be used. After addressing the Test Set, PNA sends data and is left in the state they were issued. After a read command, PNA lines AD0-AD12 are left in input mode. While in this mode the Test Set sends it address to the PNA. AD0 - AD12 are addressable with in the high power Test Set. AD0 - AD12 can be configured within the Test Set to send the PNA a unique Test Set ID.

Below is the Test Set Read/Write figure showing how the PNA communicates (hand shakes) with the Test Set. More information about The PNA Test Set I/O connector can be found in the PNA series network analyzer online Help.

Figure 24 Test Set Write

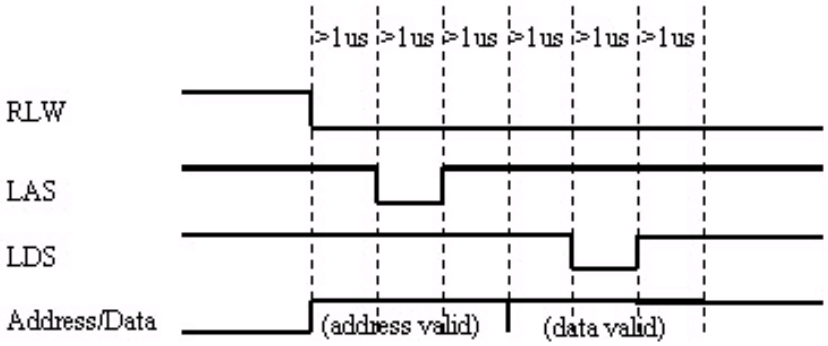
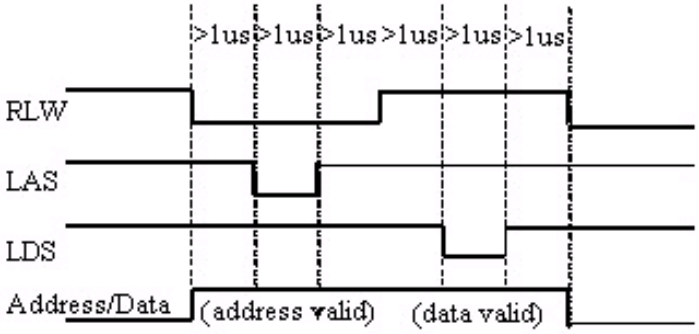


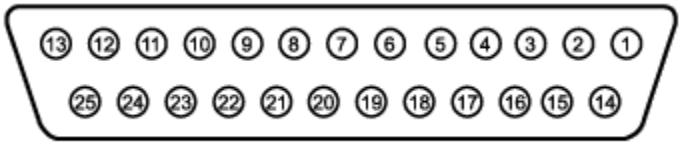
Figure 25 Test Set Read



The Test Set address depends on the input Test Set Select Bits. From the PNA, select bits are tied to ground. The first Test Set that connects to the PNA Test Set I/O connector is issued address 0. The Test Set uses these bits to determine if being addressed or not. The Test Set's Test Set Interface BD compares the select bits to the address from the PNA Test Set I/O. When the select bits match AD0-AD3 the Test Set becomes active. If the select bits do not match AD0-AD3 the Test Set is not active. The PNA address/data is 13 bits AD0-AD12. The Test Set address inputs is limited to 7 bits AD0-AD6. Address bits AD0-AD3 are dedicated to the Test Set address. Address bits AD4-AD6 determines what section the Test Set will communicate too.

The Pass Thru Interface connector on the rear panel of the Test Set passes the Address/Data, Strobes, and Interrupts from the PNA through the Test Set I/O Interface to the Pass Thru Interface. The Test Set Select bits are not directly pass through. The selected bits are received by the Test Set through the Test Set I/O Interface and incremented by the Address Val chip U40 and passed to the Pass Thru Interface. This sets the next Test Set address. Maximum number of Test Set's address allowed is 15.

Figure 26 Pass Thru Interface (J2)



Pass Thru Select Bit PSEL0, PSEL1, PSEL2, and PSEL3, Pin Numbers 1, 15, 16, 18
Pass Thru Test Set select bits; address issued by proceeding Test Set.

U40

When the Test Set's (J1) Test Set I/O Interface connector receives a command from the PNA, a Programmable Array Logic (PAL) IC U40 "Address Valid" interprets the address of the command. The Address Valid first determines if the command address AD0-AD3 matches the Select bits address. If the two address match the AOK bit goes high and signals the Test Set to be active and the address/data received is valid.

U40 also increments PSEL0-PSEL3 bits to the Pass Thru Interface. This is done by reading the Test Set I/O incoming Test Set select bits from either the PNA or Pass Thru from another Test Set.

U40 also reads AD4-AD6 when the AOK is high. A1-A4 is an address sent to the U2 "Data Valid" Programmable Array Logic (PAL) IC. This information determines what section of the Test Set Interface board is to be written too.

U41

Programmable Array Logic (PAL) IC U41 “Data Valid” interprets the address of A1-A4 and if the command is either a read or write. The Data Valid first determines if AOK is true. If AOK is true, U41 determines if the PNA is requesting or sending data to the Test Set by the state of RLW. When RLW is true the PNA is requesting information or read from the Test Set. When RLW is not true the PNA is send or writing data to the test.

The LDS provides the strobe to enable the outputs for WE1 though WE4.

When a read command is received the Data Valid PAL output pin RE enables U52 and U53 a tri-state buffer to set the AD0-AD12 data lines set by the S1 and S2 switches so the PNA can read the address. This is a unique address that the PNA can use to identify the Test Set with. This is for future use, but the address should be set so the first 8 bits AD0 through AD7 are set to decimal 83 or binary 01010011. This equals ascii character “S” for specials. The last 6 bits AD8 through AD13 will be set in binary only to indicate a order sequence the option. In this case this is the first option so the address will be set to decimal value 0 or binary 000000.

When a write command is received the Data Valid PAL A1-A4 are received and read from U40. These address lines determine what section or sections of the Test Set I/O Interface BD are to receive new information. The WE1 through WE4 are the write enable lines that enable sections 1-4. When the WE1-WE4 are high, data D0-D7 are past to the sections. WE1 enables section 1, WE2 section 2, WE3 section 3, and WE4 section 4.

U42

Programmable Array Logic (PAL) IC U42 “Data” pass eight data bits AD0-AD7 to all sections. Data is only passed when AOK is true, RLW is false, and when LDS is strobed. The outputs from this PAL are data lines D0 through D7 which are feed to sections 1-4. Currently this is being used as a latching circuit, but in the future this could be used to manipulate D I/O lines.

U43

Programmable Array Logic (PAL) IC U43 “LEDS” provides front panel stimulus. U43 deciphers AD0 through AD4 data bits along with a write enable bits WE1-WE4 to indicate the Test Set’s internal state by LEDs on the front panel.

Section 1 through 4

Sections 1 through 4 are latches. These latches hold the data when the write enable WE is false or pass the data when their corresponding WE line is true.

Section 1

Section 1 controls all J1xx switches. J101 through J106 are used for SPDT 1X2 solid-state or mechanical switches J107 and J108 are used for 1X 4 solid-state switches. J109 is used for a 50 GHZ SPDT solid-state switch.

Section 2

Section 2 controls all J200 DUT Control and J201 through J202 1X 4 solid-state switches.

Section 3 - Not Used

Section 3 controls all J3xx attenuators and switches. J300 through J303 are used for attenuators. J304 and J305 are used for 1X 4 solid-state switches.

Section 4 - Not Used

Section 4 controls all J4xx AUX switches. J401 through J406 are used for SPDT solid-state or mechanical switches J407 and J408 are used for 1X 4 solid-state switches.

Diagnostic LEDs

The PC board has several diagnostic LEDs. Each power supply has its own LED to indicate that power is present. There are also LEDs to indicate if the Test Set is being talked to, if information is being requested, and which section is to receive data. Listed below are their reference designator and description.

DS1	Address	When the Test Set address matches the command address from the PNA, the LED is On.
DS2	WE2	When data is set to section 2, the LED is On.
DS3	WE3	When data is set to section 3, the LED is On.
DS4	Read ID	When the Test Set is requested to send data back to the PNA, the LED is Off.
DS5	WE1	WE1 When data is set to section 1, the LED is On.
DS6	+5 VS	When power is connected, the LED is On.
DS7	+24 VS	When power is connected, the LED is On.
DS8	+3 VS	When power is connected, the LED is On.
DS9	+12 VS	When power is connected, the LED is On.
DS10	+15 VS	When power is connected, the LED is On.
DS11	+9 VS	When power is connected, the LED is On.
DS12	WE4	When data is set to section 4, the LED is On; currently being used as Active LED.
DS13	–12 VS	-12 VS When power is connected, the LED is On.
DS14	–9 VS	When power is connected, the LED is On.
DS16	–15 VS	When power is connected, the LED is On.

Front Panel LEDs

J30 on the Test Set I/O Interface BD connects to a ribbon cable with LEDs. These LEDs indicate the Test Set's internal state. When the LEDs are off, the Test Set is in a Bypass mode. All switches SW1-SW5 are set so the PNA is operating as a normal network analyzer. When the LEDs are all on, SW1-SW5 are set for the high power mode.

Line LED

The line LED comes ON when the front panel line switch is set to 1 position.

Active LED

The Active LED indicates if the Test Set is being talked to or that the last address was valid. When Lines WE1 through WE4 are true, then the Active LED is ON. When the PNA talks to another Test Set or if the Test Set is sent a wrong address the ACTIVE LED is OFF.

REF LED

The REF LED indicate if the Test Set SW5 is set to Bypass or High Power mode. When SW5 is in Bypass, the LED is OFF. In the high power configuration the LED is ON.

P5 LED

The P5 LED indicates if the Test Set SW1 is set to Bypass or High Power mode. When SW1 is in Bypass, the LED is OFF. In the high power configuration the LED is ON.

A LED

The A LED indicates if the Test Set SW2 is set to Bypass or High Power mode. When SW2 is in Bypass, the LED is OFF. In the high power configuration the LED is ON.

P6 LED

The P6 LED indicates if the Test Set SW3 is set to Bypass or High Power mode. When SW3 is in Bypass, the LED is OFF. In the high power configuration the LED is ON.

D LED

The D LED indicates if the test set SW4 is set to Bypass or High Power mode. When SW4 is in Bypass, the LED is OFF. In the high power configuration the LED is ON.

Safety and Regulatory Information

Introduction

Review this product and related documentation to familiarize yourself with safety markings and instructions before you operate the instrument. This product has been designed and tested in accordance with international standards.

Before Applying Power

Verify that the product is configured to match the available main power source. If this product is to be powered by autotransformer, make sure the common terminal is connected to the neutral (grounded) side of the ac power supply.

Connector Care and Cleaning

If alcohol is used to clean the connectors, the power cord to the instrument must be removed. All cleaning should take place in a well ventilated area. Allow adequate time for the fumes to disperse and moist alcohol to evaporate prior to energizing the instrument.

WARNING **To prevent electrical shock, disconnect the Agilent Technologies model Z5623A from mains before cleaning. Use a dry cloth or one slightly dampened with water to clean the external case parts. Do not attempt to clean internally.**

Compliance with Canadian EMC Requirements

This ISM device complies with Canadian ICES-001.
Cet appareil ISM est conforme a la norme NMB du Canada.

Compliance with German Noise Requirements

This is to declare that this instrument is in conformance with the German Regulation on Noise Declaration for Machines (Laermangabe nach der Maschinenlaermrerordnung-3. GSGV Deutschland).

Acoustic Noise Emission/Geraeuschemission	
LpA<70 dB	Lpa<70 dB
Operator Position	am Arbeitsplatz
Normal Operation	normaler Betrieb
per ISO 7779	nach DIN 45635 t. 19

Warnings

WARNING	**The WARNING notice denotes a hazard. It calls attention to a procedure, practice, or the like, which if not correctly performed or adhered to, could result in personal injury. Do not proceed beyond a WARNING notice until the indicated conditions are fully understood and met.**

Warnings applicable to this instrument are:

WARNING	**For continued protection against fire hazard replace line fuse only with same type and rating:** **• United States—F 5A/250V, Part Number 2110-0709** **• Europe—F 5A/250V, Part Number 2110-0709** **The use of other fuses or material is prohibited.**

WARNING	**This is a Safety Class I product (provided with a protective earthing ground incorporated in the power cord). The mains plug shall be inserted only into a socket outlet provided with a protective earth contact. Any interruption of the protective conductor, inside or outside the instrument, is likely to make the instrument dangerous. Intentional interruption is prohibited.**

WARNING	**The power cord is connected to internal capacitors that may retain dangerous electrical charges for 5 seconds after disconnecting the plug from its power supply.**

WARNING	**The opening of covers or removal of parts is likely to expose dangerous voltages. Disconnect the instrument from all voltage sources while it is being opened.**

WARNING	**If this product is not used as specified, the protection provided by the equipment could be impaired. This product must be used in a normal condition (in which all means for protection are intact) only.**

WARNING	**The detachable power cord is the instrument disconnecting device. It disconnects the mains circuits from the mains supply before other parts of the instrument. The front panel switch is only a standby switch and is not a LINE switch (disconnecting device).**

Cautions

CAUTION The CAUTION notice denotes a hazard. It calls attention to an operating procedure, practice, or the like, which if not correctly performed or adhered to, could result in damage to the product or loss of important data. Do not proceed beyond a CAUTION notice until the indicated conditions are fully understood and met.

Cautions applicable to this instrument are:

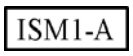
CAUTION Always use the three-prong ac power cord supplied with this instrument. Failure to ensure adequate earth grounding (by not using this cord) can cause instrument damage.

CAUTION This instrument has autoranging line voltage input; be sure the supply voltage is within the specified range.

CAUTION Ventilation Requirements: When installing the instrument in a cabinet, the convection into and out of the instrument must not be restricted. The ambient temperature (outside the cabinet) must be less than the maximum operating temperature of the instrument by 4 °C for every 100 watts dissipated in the cabinet. If the total power dissipated in the cabinet is greater than 800 watts, forced convection must be used.

CAUTION This product is designed for use in Installation Category II and Pollution Degree 2 per IEC 61010-1:2000, and 664 respectively.

Instrument Markings

	When you see this symbol on your instrument, you should refer to the instrument's instruction manual for important information.
	This symbol indicates hazardous voltages.
	The laser radiation symbol is marked on products that have a laser output.
	This symbol indicates that the instrument requires alternating current (ac) input.
	The CE mark is a registered trademark of the European Community. If it is accompanied by a year, it indicates the year the design was proven.
	The CSA mark is a registered trademark of the Canadian Standards Association.
	This symbol indicates the product meets the Australian Standards.
	This symbol indicates separate collection for electrical and electronic equipment, mandated under EU law as of August 13, 2005. All electric and electronic equipment are required to be separated from normal waste for disposal (Reference WEEE Directive, 2002/96/EC).
	This text indicates that the instrument is an Industrial Scientific and Medical Group 1 Class A product (CISPR 11, Clause 4).
	This symbol indicates that the power line switch is ON.
	This symbol indicates that the power line switch is OFF or in STANDBY position.
	Safety Earth Ground. This is a Safety Class I product (provided with a protective earthing terminal). An uninterruptible safety earth ground must be provided from the main power source to the product input wiring terminals, power cord, or supplied power cord set. Whenever it is likely that the protection has been impaired, the product must be made inoperative and secured against any unintended operation.

Contacting Agilent Sales and Service Offices

Assistance with test and measurement needs, and information on finding a local Agilent office are available on the Internet at:
http://www.agilent.com/find/assist

You can also purchase accessories or documentation items on the Internet at:
http://www.agilent.com/find

If you do not have access to the Internet, contact your field engineer.

NOTE In any correspondence or telephone conversation, refer to the product by its model number and full serial number. With this information, the Agilent representative can determine whether your unit is still within its warranty period.